**4. Counter**

**AIM:** To design and implement 3 bit UP, Down Ripple & Synchronous Counter using MS-JK Flip-flop.

**OBJECTIVE:** To understand design procedure of asynchronous & Synchronous counter.

**ICs USED :**  IC 7476 (MS-JK Flip-flop), IC 7408(Quad 2 i/p AND Gate),

IC 7432 (Quad 2 i/p OR Gate) and IC 7404 (Hex Inverter).

**THEORY:**

**Counters** : counters are logical device or registers capable of counting the no. of states or no. of clock pulses arriving at its clock input where clock is a timing parameter arriving at regular intervals of time, so counters can be also used to measure time & frequencies. They are made up of flip flops. Where the pulse are counted to be made of it goes up step by step & the o/p of counter in the flip flop is decoded to read the count to its starting step after counting n pulse incase of module counters.

**Types of Counters:**

Counter are of two types**:**

**1) Asynchronous counter.**

**2) Synchronous counter.**

**Asynchronous counter:**

A digital counter is a set of flip flop. The flip flop are connected such that their combined state at any time is binary equivalent of total no. of pulses that have occurred up to that time. Thus its name implies a counter is used to count pulse. A counter is used as frequency dividers. To obtain waveform with frequency that is specific fraction of clock frequency.

Counter may be Asynchronous or synchronous. The Asynchronous counter is also called as ripple counter .An Asynchronous counter uses T flip flop to perform a counting function. The actual hardware used is usually J-K flip flop with J & K connected to logic1. Even D flip flops may be used here.

In asynchronous counter commonly called ripple counter, the first flip-flop is clocked by the external clock pulse & then each successive flip-flop is clocked by the Q or Q’ output of the previous flip-flop. Therefore in an asynchronous counter the flip-flop’s are not clocked simultaneously. The input of MS-JK is connected to VCC because when both inputs are one output is toggled. As MS-JK is negative edge triggered at each high to low transition the next flip-flop is triggered.

**Synchronous Counter :**

When counter is clocked such that each flip flop in the counter is triggered at the same time, the counter is called as synchronous counter. The gates propagation delay at reset time will not be present or we may say will not occur.

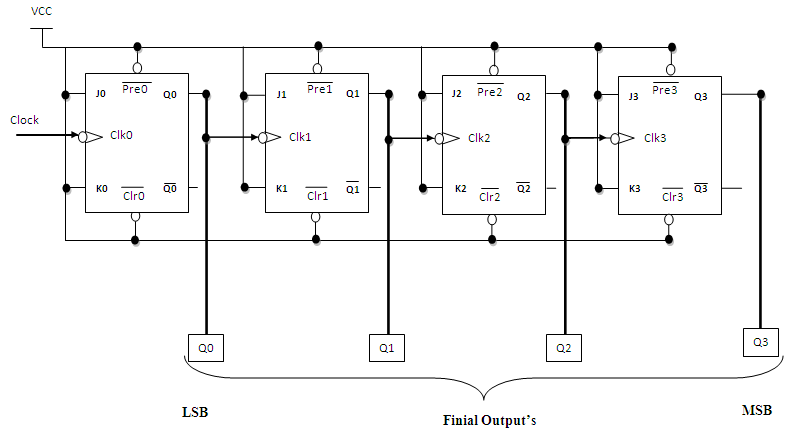
**1) Asynchronous Up Counter:**

Fig. 1 shows 3bit Asynchronous Up Counter. Here Flip-flop 2 act as a MSB Flip-flop and Flip-flop 0 act as a LSB Flip-flop. Clock pulse is connected to the Clock of Flip-flop 0. Output of Flip-flop 0(Q0) is connected to clock of next flip-flop (i.e Flip-flop 1) and so on. As soon as clock pulse changes output is going to change (at the negative edge of clock pulse) as a Up count sequence. For 3 bit Up counter state table is as shown below.

|  |  |  |  |
| --- | --- | --- | --- |
| Counter States | Count | | |
| Q2 | Q1 | Q0 |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |

**State Table :**

**Logic diagram :**

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**Fig 1: 3 Bit Asynchronous Up Counter**

**Hardware requirements :**

|  |  |  |  |
| --- | --- | --- | --- |
| **Gate /**  **Flip flop** | **Quantity** | **IC** | **Quantity** |
| MS JK | 3 | 7476 | 2 |

**2) Down Counter:**

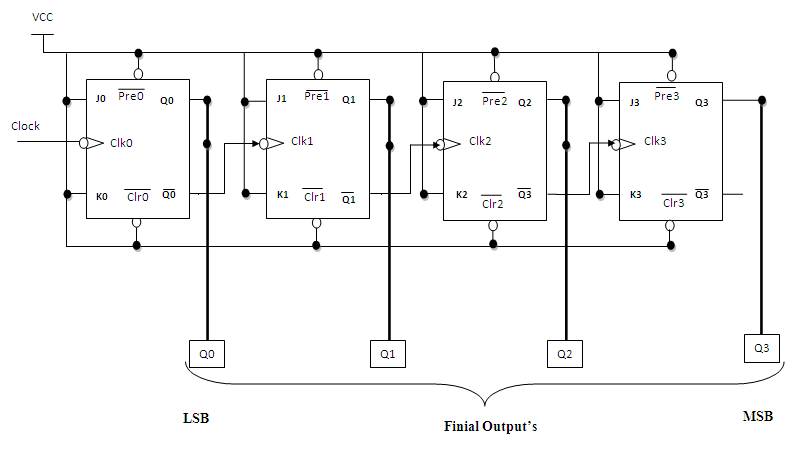
Fig. 2 shows 2 bit Asynchronous Down Counter. Here Flip-flop 2 act as a MSB Flip-flop and Flip-flop 0 act as a LSB Flip-flop. Clock pulse is connected to the Clock of Flip-flop 0. Output of Flip-flop 0 (Q0’) is connected to clock of next flip-flop (i.e Flip-flop 1) and so on. As soon as clock pulse changes output is going to change (at the negative edge of clock pulse) as a down count sequence. For 3 bit down counter sate table is as shown below.

In both the counters Inputs J and K are connected to Vcc, hence J-K Flip flop work in toggle mode. Preset and Clear both are connected to logic 1.

|  |  |  |  |
| --- | --- | --- | --- |
| Counter States | Count | | |
| Q2 | Q1 | Q0 |
| 7 | 1 | 1 | 1 |
| 6 | 1 | 1 | 0 |
| 5 | 1 | 0 | 1 |
| 4 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 |
| 7 | 1 | 1 | 1 |

**State Table :**

**Logic diagram :**

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**Fig 2: 3 Bit Asynchronous Down Counter**

**Hardware requirements :**

|  |  |  |  |
| --- | --- | --- | --- |
| **Gate /**  **Flip flop** | **Quantity** | **IC** | **Quantity** |
| MS JK | 3 | 7476 | 2 |

Applications **:**

The asynchronous counters are specially used as the counting devices.

They are also used to count number of pulses applied.

It also works as frequency divider.

It helps in counting the number of product coming out of the machinery where product is coming out at equal interval of time.

**Types of synchronous counter:**

**1) Up counter.**

**2) Down counter.**

**1. 3 bit Synchronous up counter:**

The up counter counts from 0 to7 i.e.(000 to 111).for this we are using MS JK flip flop. In IC 74LS76, 2 MS J-K flip flops are present. The clock pulse is given at pin 1 & 6 of the 1st IC & pin 1 of 2nd IC. Next state decoder logic is designed with the help of state table.

**State table for synchronous up counter:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Present state** | | | **Next state** | | | **Flip flop 3** | | **Flip flop 2** | | **flip flop 1** | |
| **Q2** | **Q1** | **Q0** | **Q2** | **Q2** | **Q0** | **J2** | **K2** | **J1** | **K1** | **J0** | **K0** |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | x | 0 | X | 1 | x |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | x | 1 | X | x | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | x | x | 0 | 1 | x |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | x | x | 1 | x | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | x | 0 | 0 | X | 1 | X |
| 1 | 0 | 1 | 1 | 1 | 0 | x | 0 | 1 | X | x | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | x | 0 | x | 0 | 1 | X |
| 1 | 1 | 1 | 0 | 0 | 0 | x | 1 | x | 1 | x | 1 |

**K-Map :**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | 0 | 0 | 1 | 0 |
| **1** | X | X | X | X |

**J2 = Q1Q0**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | X | X | X | X |
| **1** | 0 | 0 | 1 | 0 |

**K2 = Q1Q0**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | 0 | 1 | X | X |
| **1** | 0 | 1 | X | X |

**J1 = Q0**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | X | X | 1 | 0 |
| **1** | X | X | 1 | 0 |

**K1 = Q0**

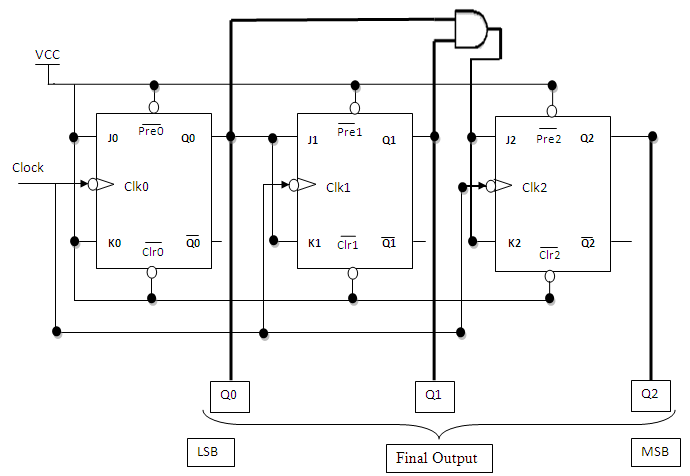
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | 1 | X | X | 1 |
| **1** | 1 | X | X | 1 |

**J0 = 1**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | X | 1 | 1 | X |
| **1** | X | 1 | 1 | X |

**K0 = 1**

**Logic Diagram:**

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**Fig 1: 3 bit Synchronous up counter**

**2. 3 bit Synchronous down counter:**

This is used to count from 7-0 i.e.(111-000).for this also 2 IC’s of 74LS76 are required & hence we use 3 MS JK flip flops. Here also clock is given to 1st & 6th pin of 1st IC & 1st pin of 2nd IC enabling to apply clock to all flip flop at a time. Next state decoder logic is designed with the help of state table.

**State table for synchronous down counter :**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Present state** | | | **Next state** | | | **Flip flop 3** | | **Flip flop 2** | | **Flip flop 1** | |
| **Q2** | **Q1** | **Q0** | **Q2** | **Q1** | **Q0** | **J2** | **K2** | **J1** | **K1** | **J0** | **K0** |
| **1** | **1** | **1** | **1** | **1** | **0** | **X** | **0** | **X** | **0** | **X** | **1** |
| **1** | **1** | **0** | **1** | **0** | **1** | **X** | **0** | **X** | **1** | **1** | **X** |
| **1** | **0** | **1** | **1** | **0** | **0** | **X** | **0** | **0** | **X** | **X** | **1** |
| **1** | **0** | **0** | **0** | **1** | **1** | **X** | **1** | **1** | **X** | **1** | **X** |
| **0** | **1** | **1** | **0** | **1** | **0** | **0** | **X** | **X** | **0** | **X** | **1** |
| **0** | **1** | **0** | **0** | **0** | **1** | **0** | **X** | **X** | **1** | **1** | **X** |
| **0** | **0** | **1** | **0** | **0** | **0** | **0** | **X** | **0** | **X** | **X** | **1** |
| **0** | **0** | **0** | **1** | **1** | **1** | **1** | **X** | **1** | **X** | **1** | **X** |

**K-Map :**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | 1 | 0 | 0 | 0 |
| **1** | X | X | X | X |

**J2 = Q1 Q0**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | X | X | X | X |
| **1** | 1 | 0 | 0 | 0 |

**K2 = Q1 Q0**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | 1 | 0 | X | X |
| **1** | 1 | 0 | X | X |

**J1 = Q0**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | X | X | 0 | 1 |
| **1** | X | X | 0 | 1 |

**K1 = Q0**

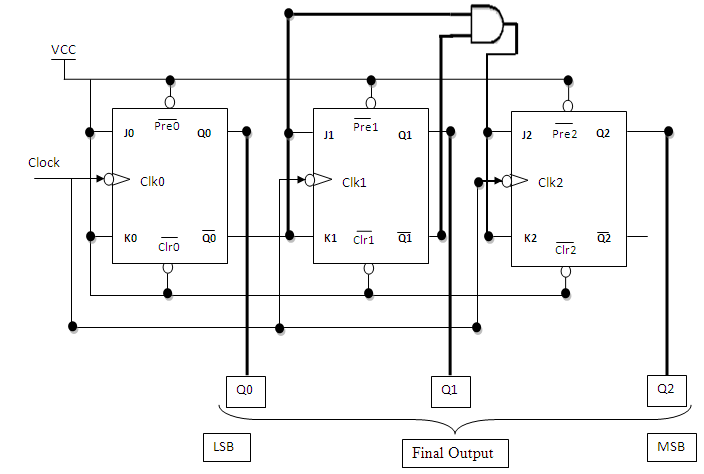
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | 1 | X | X | 1 |
| **1** | 1 | X | X | 1 |

**J0 = 1**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1Q0**  **Q2** | **00** | **01** | **11** | **10** |
| **0** | X | 1 | 1 | X |
| **1** | X | 1 | 1 | X |

**K0 = 1**

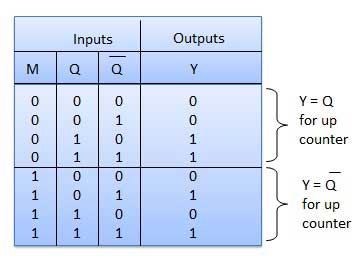
**Logic Diagram :**



**Fig 2: 3 bit Synchronous down counter**

**3-Bit Asynchronuous up/down counter with Mode Control input M**

**Truth Table**



**K map**

**Circuit Diagram**

**3-Bit Synchronuous up/down counter with Mode Control input M**

**Truth Table**

**Kmap**

**Circuit Diagram**

**Uses:**

1. Specially used as the counting devices.
2. Used in frequency divider circuit.
3. Used in digital voltmeter.
4. Used in counter type A to D converter.
5. Used for time measurement..
6. It helps in counting the no of product coming out from machinery where product is coming out at equal interval of time.

**Conclusion:**

Up and down counters are successfully implemented, the counters are studied & o/p are checked. The state table is verified.

**PRACTICE ASSIGNMENTS / EXERCISE / MODIFICATIONS:**

1. Design & implement 2 bit controlled synchronous counter.

2. Design & implement 4 bit controlled synchronous counter.

3. Design & implement truncated synchronous up or down counter.

**FAQ’s with answers:**

1. What do you mean by Counter?

A Counter is a register capable of counting the no. of clock pulses arriving at its

clock inputs. Count represents the no. of clock pulses arrived. A specified

sequence of states appears as the counter output.

1. What are the types of Counters? Explain each.

There are two types of counters as Asynchronous Counter and Synchronous Counter. Asynchronous Counter: In this counter, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the Q or Q’ o/p of the previous flip-flop. Hence in Asynchronous Counter flip-flops are not clocked simultaneously and hence called as Ripple Counter. Synchronous Counter: In this counter, the common clock input is connected to all the flip-flops simultaneously.

1. What do you mean by pre-settable counters?

A counter in which starting state is not zero can be designed by making use of the

preset inputs of the flip flops. This is referred to as loading the counter

asynchronously. This is referred to as pre-settable counter.

1. What are the applications of synchronous counters?

Digital clock

Frequency divider circuits

Frequency counters

Used in analog to digital converters

1. What are the advantages of synchronous counters over asynchronous counters?

Propagation delay time is reduced.

Can operate at a much higher frequency than the asynchronous counters.

1. Ring counter is an example of synchronous counters or asynchronous counter?

Synchronous counter. Since all the flip flops are clocked simultaneously.

1. Twisted Ring (Johnson’s) counter is an example of synchronous counters or asynchronous counter?

Synchronous counter. Since all the flip flops are clocked simultaneously.

1. What is the difference between ring counter and twisted ring counter?

In ring counter pulses to be counted are applied to a counter , it goes from state to state and the output of the flip flop s in the counter is decoded to read the count. Here the uncomplimentary output (Q) of last flip flop is fed back as an input to first flip flop. Ring counters are referred as MOD ‘N’ counters.

But in Twisted ring counter the complimentary output (Q bar) of last flip flop is fed back as an input to first flip flop. Twisted Ring counters are referred as MOD ‘2N’ counters.

1. What are the applications of ring counters?

Ring counter outputs are sequential non-overlapping pulses which are useful for control state counters, Used in stepper motor, this requires pulses to rotate it from one position to the next. Used as divide by ‘N’ ((MOD ‘N’) counters.

1. What are the applications of ring counter twisted ring counters?

Used as divide by ‘2N’ ((MOD ‘2N’) counters.

Used for control state counters.

Used for generation of multiphase clock.

1. List the Synchronous Counter ICs.

IC 74160 : Decade Up Counter

IC 74161 : 4 bit binary Up Counter

IC 74162 : Decade Up Counter

IC 74163 : 4 bit binary Up Counter

IC 74168 : Decade Up/Down Counter

IC 74169 : 4 bit Binary Up/Down Counter

IC 74190 : Decade Up/Down Counter

IC 74191 : 4 bit Binary Up/Down Counter

IC 74192 : Decade Up/Down Counter

IC 74193 : 4 bit Binary Up/Down Counter